AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor device comprising:

a TFT formed over a substrate;

an active layer formed in the TFT; and

a first region, a second region and a third region formed in the active layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a carrier flow direction,

wherein a portion of the third region is convexed or concaved in the direction perpendicular to the carrier flow direction, which is parallel to a plane of the substrate, the convexed portion being a part of the second width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero, and

wherein the first width is narrower than the second width.

2. (Currently amended) A semiconductor device comprising:

a TFT formed over a substrate;

an active layer formed in the TFT; and

a first region, a second region and a third region formed in the active layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a carrier flow direction,

wherein a portion of the third region is convexed or concaved in the direction perpendicular to the carder flow direction, which is parallel to a plane of the substrate, the convexed portion being a part of the second width.

wherein ~~zero or one~~ the number of grain boundary [[is]] contained in the channel forming region is zero, and

wherein the first width is narrower than the second width.

3. (Currently amended) A semiconductor device comprising:

a TFT formed over a substrate;

an active layer formed in the TFT; and

a first region, a second region and a third region formed in the active layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a carrier flow direction,

wherein a portion of the third region is convexed or concaved in the direction perpendicular to the carrier flow direction, which is parallel to a plane of the substrate, the convexed portion being a part of the second width,

wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is ~~zero or~~ one, [[and]]

wherein the one grain boundary is not overlapped with the convexed or concaved portion in the width direction of the channel forming region, and

wherein the first width is narrower than the second width.

4. (Withdrawn) A method of manufacturing a semiconductor device, comprising the steps of:

forming a semiconductor film over a substrate;

forming a crystalline semiconductor film by irradiating a laser light to said semiconductor film;

forming a convex portion or a concave portion in a region which is a portion of said crystalline semiconductor film and which later contains a channel forming region; and

irradiating the laser light to said crystalline semiconductor film in which the convex portion or the concave portion is formed.

5. (Withdrawn) A method of manufacturing a semiconductor device, comprising the steps of:

forming a semiconductor film over a substrate;

forming a crystalline semiconductor film by irradiating a laser light to said semiconductor film;

forming a convex portion or a concave portion in a region which is a portion of said crystalline semiconductor film and which later contains a channel forming region; and

irradiating the laser light to the top surface and to the bottom surface of said crystalline semiconductor film in which the convex portion or the concave portion is formed.

6. (Withdrawn) A method of manufacturing a semiconductor device, comprising the steps of;

forming a semiconductor film over a substrate;

forming semiconductor islands by patterning said semiconductor film, each of said semiconductor island having a convex portion or a concave portion in a region which later contains a channel forming region, and

crystallizing said semiconductor islands by irradiating a laser light.

7. (Withdrawn) A method of manufacturing a semiconductor device, comprising the steps of:

forming a semiconductor film over a substrate;

forming semiconductor islands by patterning said semiconductor film, each of said semiconductor island having a convex portion or a concave portion in a region which later contains a channel forming region, and

crystallizing said semiconductor islands by irradiating a laser light to the top surface and to the bottom surface thereof.

8. (Withdrawn) The method of manufacturing a semiconductor device according to claim 5, wherein a relationship of $0 < (I_0' / I_0) < 1$, or a relationship of $1 < (I_0' / I_0)$, exists between the effective energy strength of the laser light irradiated on the top surface of said semiconductor film (I_0) and the effective energy strength of the laser light irradiated on the bottom surface of said semiconductor film (I_0').

9. (Withdrawn) The method of manufacturing a semiconductor device according to claim 7, wherein a relationship of $0 < (I_0' / I_0) < 1$, or a relationship of $1 < (I_0' / I_0)$, exists between the effective energy strength of the laser light irradiated on the top surface of said semiconductor island (I_0') and the effective energy strength of the laser light irradiated on the bottom surface of said semiconductor island (I_0).

10. (Previously Presented) A semiconductor device according to any one of claims 1 to 3, wherein said semiconductor device is incorporated into an electronic device selected from the group consisting of a personal computer, a projector, a digital camera, a video camera, a head mounted display, a portable information terminal, a navigation system, a game machine, an image playback machine and a music playback machine.

11. (Currently amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate; and

a first region, a second region and a third region formed in the semiconductor layer, the third region being formed between the first region and the second region, wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a channel length direction,

wherein a portion of the third region is convexed in the direction perpendicular to the channel length direction and parallel to a plane of the substrate, the convexed portion being a part of the second width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero, and

wherein the first width is narrower than the second width.

12. (Currently amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate; and

a first region, a second region and a third region formed in the semiconductor layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a channel length direction,

wherein a portion of the third region is concaved in the direction perpendicular to the channel length direction and parallel to a plane of the substrate, the channel forming region including the concaved portion and having the first width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero, and

wherein the first width is narrower than the second width.

13. (Currently amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate; and

a first region, a second region and a third region formed in the semiconductor layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a channel width direction,

wherein a portion of the third region is convexed in the channel width direction, the channel width direction being parallel to a plane of the substrate, the convexed portion being a part of the second width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in the width direction of the channel forming region is one,

wherein the one grain boundary is not overlapped with the convexed portion in the width direction of the channel forming region, and

wherein the first width is narrower than the second width.

14. (Currently amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate; and

a first region, a second region and a third region formed in the semiconductor layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a channel width direction,

wherein a portion of the third region is concaved in the channel width direction, the channel width direction being parallel to a plane of the substrate, the channel forming region including the concaved portion and having the first width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in the width direction of the channel forming region is one,

wherein the one grain boundary is not overlapped with the concaved portion in the width direction of the channel forming region, and

wherein the first width is narrower than the second width.

15. (Currently amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate; and

a first region, a second region and a third region formed in the semiconductor layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a carrier flow direction,

wherein a portion of the third region is convexed in the direction perpendicular to the carrier flow direction and parallel to a plane of the substrate, the convexed portion being a part of the second width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero, and

wherein the first width is narrower than the second width.

16. (Currently amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate; and

a first region, a second region and a third region formed in the semiconductor layer, the third region being formed between the first region and the second region,

wherein the third region includes a channel forming region,

wherein the third region has a first width and a second width,

wherein the first width and the second width of the third region are narrower than a width of the first region and a width of the second region,

wherein each of the first width and the second width of the third region, the width of the first region and the width of the second region is a length in a direction perpendicular to a carrier flow direction,

wherein a portion of the third region is concaved in the direction perpendicular to the carrier flow direction and parallel to a plane of the substrate, the channel forming region including the concaved portion and having the first width, [[and]]

wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero, and

wherein the first width is narrower than the second width.

17. (Previously Presented) A semiconductor device according to any one of claims 11-16, wherein said semiconductor device is incorporated into an electronic device selected from the group consisting of a personal computer, a projector, a digital camera, a video camera, a head mounted display, a portable information terminal, a navigation system, a game machine, an image playback machine and a music playback machine.

18-20. (Canceled)

21. (Previously Presented) A semiconductor device according to claim 11, wherein the channel length direction is parallel to a direction in which a carrier flows from the first region to the second region.

22. (Previously Presented) A semiconductor device according to claim 12, wherein the channel length direction is parallel to a direction in which a carrier flows from the first region to the second region.

23. (Previously Presented) A semiconductor device according to claim 13, wherein the channel width direction is perpendicular to a direction in which a carrier flows from the first region to the second region.

24. (Previously Presented) A semiconductor device according to claim 14, wherein the channel width direction is perpendicular to a direction in which a carrier flows from the first region to the second region.

25. (Previously Presented) A semiconductor device according to claim 11, wherein zero or one grain boundary is contained in the channel forming region.

26. (Previously Presented) A semiconductor device according to claim 12, wherein zero or one grain boundary is contained in the channel forming region.

27. (Previously Presented) A semiconductor device according to claim 13, wherein zero or one grain boundary is contained in the channel forming region.

28. (Previously Presented) A semiconductor device according to claim 14, wherein zero or one grain boundary is contained in the channel forming region.

29. (Previously Presented) A semiconductor device according to claim 15, wherein zero or one grain boundary is contained in the channel forming region.

30. (Previously Presented) A semiconductor device according to claim 16, wherein zero or one grain boundary is contained in the channel forming region.

31. (Previously Presented) A semiconductor device according to claim 11, wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero or one.

32. (Previously Presented) A semiconductor device according to claim 12, wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero or one.

33. (Previously Presented) A semiconductor device according to claim 13, wherein the number of grain boundaries crossing the channel forming region in the channel width direction is zero or one.

34. (Previously Presented) A semiconductor device according to claim 14, wherein the number of grain boundaries crossing the channel forming region in the channel width direction is zero or one.

35. (Previously Presented) A semiconductor device according to claim 15, wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero or one.

36. (Previously Presented) A semiconductor device according to claim 16, wherein the number of grain boundaries crossing the channel forming region in a width direction of the channel forming region is zero or one.

37. (Previously Presented) A semiconductor device according to claim 1, wherein the first region includes a source region and the second region includes a drain region.

38. (Previously Presented) A semiconductor device according to claim 2, wherein the first region includes a source region and the second region includes a drain region.

39. (Previously Presented) A semiconductor device according to claim 3, wherein the first region includes a source region and the second region includes a drain region.

40. (Previously Presented) A semiconductor device according to claim 11, wherein the first region includes a source region and the second region includes a drain region.

41. (Previously Presented) A semiconductor device according to claim 12, wherein the first region includes a source region and the second region includes a drain region.

42. (Previously Presented) A semiconductor device according to claim 13, wherein the first region includes a source region and the second region includes a drain region.

43. (Previously Presented) A semiconductor device according to claim 14, wherein the first region includes a source region and the second region includes a drain region.

44. (Previously Presented) A semiconductor device according to claim 15, wherein the first region includes a source region and the second region includes a drain region.

45. (Previously Presented) A semiconductor device according to claim 16, wherein the first region includes a source region and the second region includes a drain region.